ISL59444EVAL1 Evaluation Board User's Guide

Application Note | April 19, 2005 | AN1184.0

Introduction

The ISL59444EVAL1 evaluation board contains all the circuitry needed to characterize critical performance parameters of the ISL59444 single 4:1 MUX-amplifier, over a variety of applications.

The ISL59444 is a single-output 4:1 MUX-amps with a unity-gain bandwidth of 1GHz. The device contains logic inputs for channel selection (S0, S1) three-state output control (HIZ) that allows individual selection of MUX amps that share a common video output line. Latches $\overline{LE1}$ and $\overline{LE2}$ provide synchronous switching of the channel select logic to the output.

The evaluation board circuit and layout is optimized for either 50Ω or 75Ω terminations, and implements a basic single 4:1 video MUX-amp. The board is supplied with 75Ω input signal terminations and a 75Ω back-termination resistor on each of the 3 outputs, making it suitable for driving video cable. The user has the option of replacing the 75Ω resistors with 50Ω resistors for other applications. The control lines contain 50Ω resistors to match the 50Ω output impedance of high speed pulse generators. Control line termination resistors are recommended for rise and fall times under 10ns to minimize unwanted transients. If DC is used for the control logic, the resistors may be removed; or the applied DC voltage can be reduced to 2.5V to reduce the dissipation in the termination resistor.

The layout contains component options to include an output series resistor (R_S) followed by a parallel resistor (R_L) capacitor (C_L) network to ground. This option allows the user to select several different output configurations. Examples are shown in Figures 3A, 3B, and 3C. The evaluation board is supplied with the 75Ω back termination resistors shown in Figure 3C.

Amplifier Performance and Output Configurations

The ISL59444 output amplifier is sensitive to capacitance at the output. For best AC performance, a series output resistor is required to reduce excessive gain peaking, particularly when long PB board traces are used. The output amplifier is ideally suited for driving high impedance high speed selectable-gain buffers when gain compensation is needed. GBW decreases slightly at the lower output load impedances typical of back-terminated cable driving applications. Reference data sheets for additional performance data.

High Frequency Layout Considerations

At frequencies of 500MHz and higher, circuit board layout may limit performance. The following layout guidelines are implemented on the evaluation board:

- Signal I/O lines are the same lengths and widths to match propagation delay and trace parasitics.
- No series connected vias are used in signal I/O lines, as they can add unwanted inductance.
- Signal trace lengths are minimized to reduce transmission line effects and the need for strip-line tuning of the signal traces.
- High frequency decoupling caps are places as close to the device power supply pin as possible - without series vias between the capacitor and the device pin.

Power Sequencing

Proper power supply sequencing is -V first, then +V. In addition, the +V and -V supply pin voltage rate-of-rise must be limited to ±1V/µs or less. The evaluation board contains parallel-connected low V_{ON} Schottky diodes on each supply terminal to minimize the risk of latch up due to incorrect sequencing. In addition, extra 10µF decoupling capacitors are added to each supply to aid in reducing the applied voltage rate-of-rise.

Reference Documents

- ISL59444 Data Sheet, FN7451

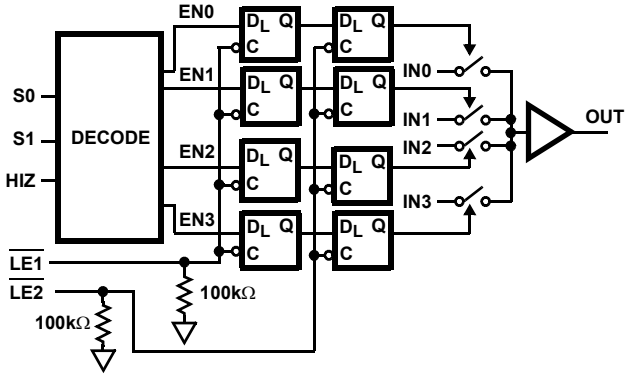


FIGURE 1. ISL59444 FUNCTIONAL BLOCK DIAGRAM

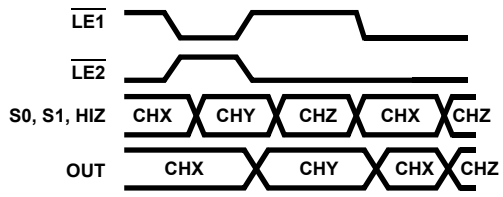
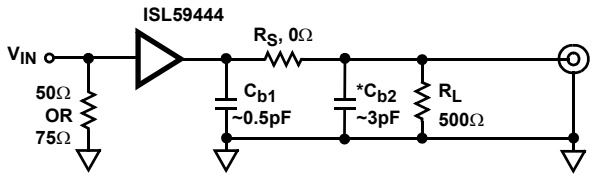


FIGURE 2. ISL59444 TIMING DIAGRAM

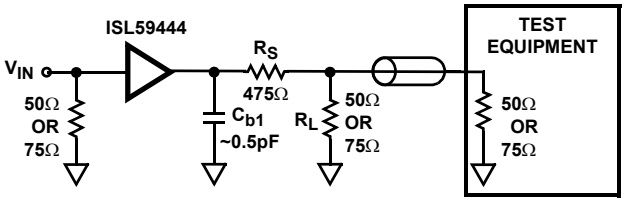
TABLE 1. LOGIC TABLE

S0	S1	$\overline{LE1}/\overline{LE2}$	HIZ	OUT
0	0	0	0	IN0
1	0	0	0	IN1
0	1	0	0	IN2
1	1	0	0	IN3
-	-	0	1	High Z
-	-	Timing Diagram	0	Timing Diagram



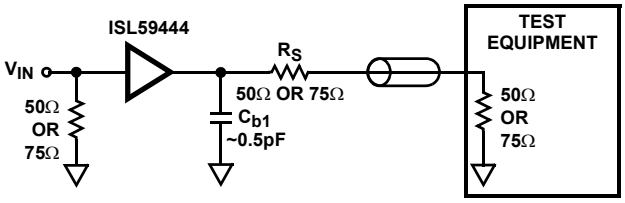
* C_{b1}, C_{b2} are approximate PCB trace capacitances.

FIGURE 3A. TEST CIRCUIT WITH OPTIMAL OUTPUT LOAD



* C_{b1} is approximate PCB trace capacitance.

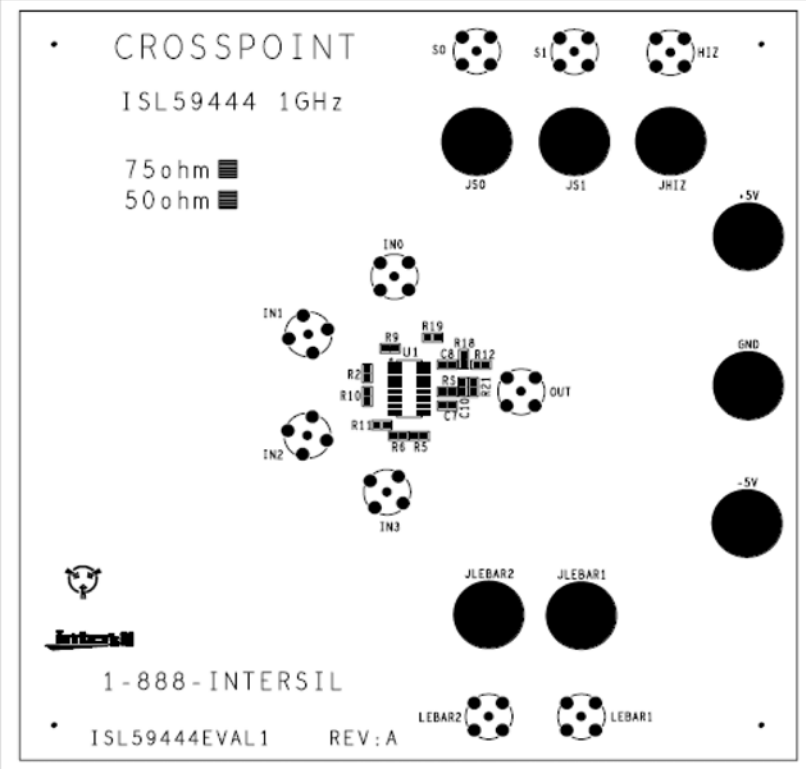
FIGURE 3B. TEST CIRCUIT FOR 50Ω OR 75Ω TERMINATIONS



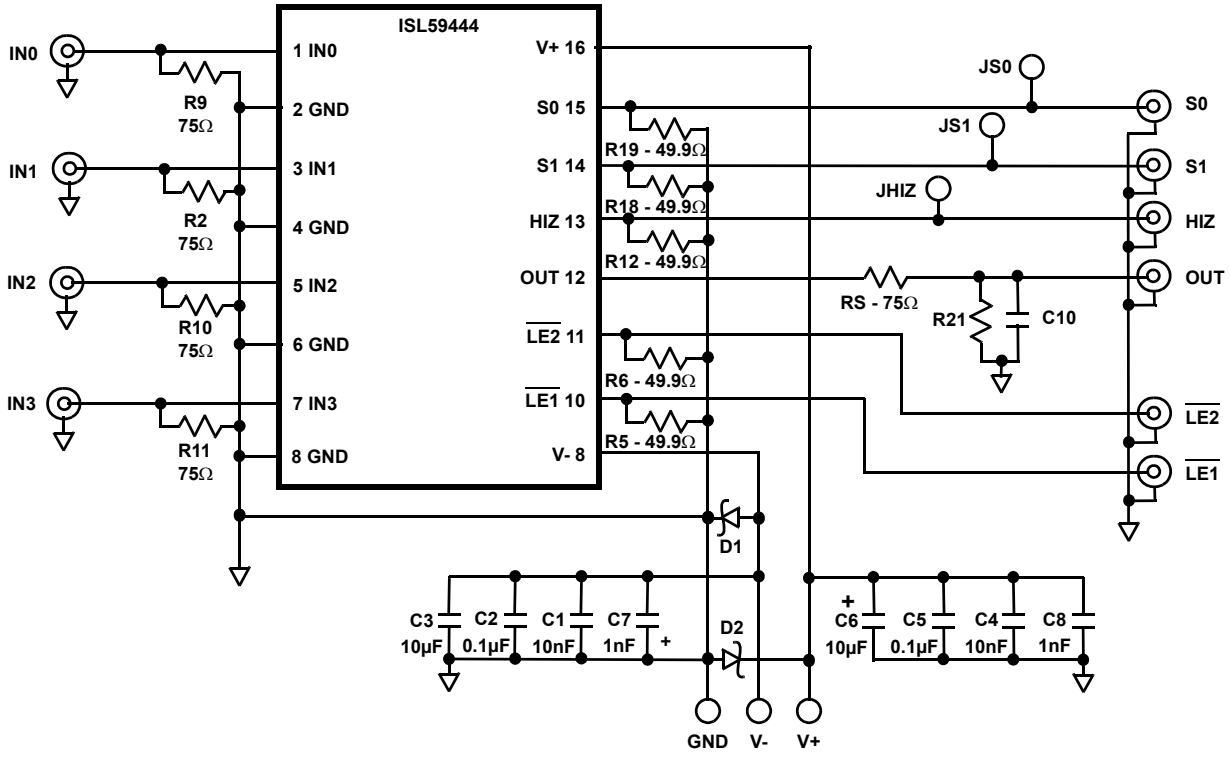
* C_{b1} is approximate PCB trace capacitance.

FIGURE 3C. BACK-TERMINATED TEST CIRCUIT FOR CABLE APPLICATION

ISL59444EVAL1 Top View



ISL59444EVAL1 Schematic Diagram



ISL59444EVAL1 Components Parts List

DEVICE #	DESCRIPTION	COMMENTS
C7, C8	CAP, SMD, 0603, 1000pF, 25V, 10%, X7R	Power Supply Decoupling
C1, C4	CAP, SMD, 0603, 0.01µF, 25V, 10%, X7R	Power Supply Decoupling
C2, C5	CAP, SMD, 0603, 0.1µF, 25V, 10%, X7R	Power Supply Decoupling
C3, C6	CAP, SMD, 0805, 10µF, 6.3V, 10%, X5R	Power Supply Decoupling
D1, D2	Diode-Schottky, 2 Pin, 45V, 7.5A	MBR0550T (Motorola) Reverse Polarity Protection
R2, R9, R10, R11, RS	Resistor, SMD, 0603, 75Ω, 1/10W, 1%	Signal Input/output Termination
R5, R6, R12, R18, R19	Resistor, SMD, 0603, 49.9Ω, 1/16W, 1%	Logic Input Termination
C10	Resistor, SMD, 0603	Optional, not populated
R21	Resistor, SMD, 0603	Optional, not populated
U1	ISL59444 - 1GHz Multiplexing Amplifier, 16P, QSOP	Device Under Test